

BIO - DATA

Name : G.BABU
Designation : LECTURER
Department : ELECTRONICS AND COMMUNICATION ENGINEERING
Employee ID : 1250648
Date of Birth : 25-07-1987
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Address for Communication: mallela,thondur(m),kadapa(Dist.)

Date of Initial appointment in the department: 16-10-2013

Date of joining at this institute: 13-01-2022

Total Experience: 16 years

Educational Qualifications:

S.No.	Degree	University/Board/Institution	Year of Passing
1	Ph.D	JNTUA,Ananthapuramu	Pursuing
2	M.Tech	JNTUA,Ananthapuramu	2018
3	B.Tech	S.V.U	2008
4	Diploma	GPT Ananthapur,SBTET	2005

Details of Experience:

S.No.	Name of the Institution/Organization	Designation	From	To
1.	BSNL	Junior Engineer	20-06-2009	31-06-2011
2	Indian Railways	Sr. Section Engineer	01-07-2011	14-10-2013
3.	GPT Vempalli	Lecturer	16-10-2023	13-01-2022
4.	GPT Proddatur	Lecturer	13-01-2022	Till date

Training Details:

S.No.	Name of the Programme	Conducted by	Duration and Dates
1.	Circuits and Measurements Lab Practice	NITTTR Chennai	16-02-2015 to 20-02-2015 (one week)
2	Advanced Communications	NITTTR Chennai	27-06-2016 to 01-07-2016 (one week)
3.	Circuit simulation and PCB design using Multisim	NITTTR Chennai	01-08-2016 to 05-08-2016 (one week)
4.	Special electrical machines and control	NITTTR Chennai	29-01-2018 to 02-02-2018 (one week)
5.	Induction Programme for newly	NITTTR Chennai	16-04-2018 to 27-04-

	recruited Teachers		2018 (two weeks)
6.	Laboratory Instruction in communication	NITTTR Chennai	27-05-2019 to 01-06-2019 (one week)
7.	Refresher Course on Electronics	NITTTR Chennai	11-11-2019 to 22-11-2019 (two weeks)
8.	Laboratory Practice in Pspice	NITTTR Chennai	28-03-2022 to 01-04-2022 (one week)
9.	Embedded System Design and development	NITTTR Chennai	30-10-2023 to 03-11-2023 (one week)
10.	Design of smart digital IC by using Cadence	CITD,Hyderabad	22-01-2024 to 10-02-2024 (three weeks)
11.	Three weeks industrial training for faculty	ECIL,Hyderabad	19-08-2024 to 06-09-2024 (three weeks)
12.	System Design Through Verilog	NPTEL	Jul-Sep-2024

Signature